ELECTROLESS Ni/Pd/Au METALLIZATION STRUCTURE FOR COPPER INTERCONNECT SUBSTRATE AND METHOD THEREFOR

Manufacturers of semiconductor integrated circuits have been experimenting with the use of copper to form the interconnect metallization upon integrated circuits. Copper has much better conductivity than the traditional aluminum metallization that has been used in past years, and improved conductivity is essential to achieve higher speed operation.

Such integrated circuits typically have a series of electrical connection pads by which the integrated circuit can be electrically joined with other external circuitry. For example, wire bonds have long been used to electrically couple the connection pads of an integrated circuit to the leads of a package, or to a supporting substrate. Solder bumps are also a cost-effective, and convenient, method of electrically coupling integrated circuits to supporting substrates within an electronics system; such solder bumps are often formed on integrated circuit wafers of the type that are used in providing so-called flip chip integrated circuit packages and/or chip scale packages.

Traditional wire bond and solder bumping methods cannot be used reliably with integrated circuits using copper interconnect metallization. In the case of gold wire bonds, an interaction takes place between the gold of the gold wire bond and the very thin copper layer to which it is bonded, and this interaction degrades the performance and reliability of the copper layer. Likewise, in the case of solder balls, an interaction takes place between the Sn/Pb solder and the very thin copper layer to which the solder is applied, and this interaction similarly degrades the performance and reliability of the copper layer. In addition, solder bumps require a solder diffusion barrier between the solder and the final copper metal of the integrated circuit. Others have proposed the use of nickel to serve as a bridge and barrier between the copper and gold in various applications. However, in many cases, integrated circuit die must be thermal cycled either at the wafer level (i.e., prior to scribing the die), or at the individual die level (after the wafer is scribed and the die are "broken" apart from the wafer), before the integrated circuit is finally assembled. Such thermal cycling steps could include wire bonding, die attachment, and wafer-level burn-in used to detect marginal Ics. In some cases, such thermal cycling is conducted in order to eliminate defects within, and improve the

performance of, transistors and other devices formed within such integrated circuits, as by releasing trapped charges from the semiconductor devices (FETs, etc.) that are part of the integrated circuits. The heating associated with such thermal cycling tends to cause the nickel material to diffuse outwardly into the gold wire or solder bump, and such outward diffusion weakens the joint between the gold wire bond, or the solder bump, and the integrated circuit connection pad.

As is well known, integrated circuits are typically fabricated from semiconductor wafers in which a relatively large number of such identical integrated circuits are fabricated at once. Once the wafer level processing of such semiconductor wafers is complete, the wafers are scribed and broken along the scribe lines to form individual integrated circuit die. Clearly, it is an advantage to perform required processes at the wafer level, rather than at the individual circuit die level, as costs are thereby minimized.

Accordingly, it is an object of the present invention to provide an integrated circuit structure at the wafer level which makes use of copper interconnect metallization while facilitating the electrical coupling of connection pads of the integrated circuits to supporting substrates or other packaging.

Another object of the present invention is to provide such an integrated circuit structure using known metal deposition processes in a simple and inexpensive manner.

Still another object of the present invention is to provide such an integrated circuit structure which is compatible with gold wire bonds, solder bumps, and other common circuit connection methods.

A further object of the present invention is to provide such an integrated circuit structure capable of permitting relatively tight spacings between adjacent connection pads without compromising the reliability of the integrated circuit.

Yet another object of the present invention is to provide a process for forming connection pads on a plurality of integrated circuit die formed in semiconductor wafer, wherein the process is compatible with copper interconnect metallization while facilitating the use of gold wire bonds, solder bumps, and other common methods for electrically interconnecting the electrodes of an integrated circuit to a supporting substrate or packaging.

These and other objects of the present invention will become more apparent to those skilled in the art as the description of the present invention proceeds.

Summary of the Invention

Briefly described, and in accordance with a preferred embodiment thereof, the present invention relates to an integrated circuit structure that includes a semiconductor wafer having a number of integrated circuit die formed therein, each having a series of semiconductor devices formed therein upon one surface of the semiconductor wafer. A patterned layer of interconnect metal, preferably formed of copper, is formed upon the upper surface of the semiconductor wafer for electrically interconnecting the various semiconductor devices formed within each such die. The patterned interconnect metal layer includes connection pads for making electrical connection to external circuitry. A patterned layer of nickel is plated, preferably by an electroless plating process, over each connection pad for mechanically and electrically bonding to the interconnect metal forming such connection pad. A patterned layer of palladium is then plated, preferably by an electroless plating process, over the previously-applied layer of nickel above each connection pad for preventing the nickel from out-diffusing during subsequent thermal cycling to a patterned gold layer that is applied over the palladium layer. Thereafter, the patterned layer of gold is plated, again preferably by an electroless plating process, over the patterned layer of palladium above each connection pad to facilitate the joinder of such connection pad with a connection element, such as a gold wire bond, solder bump, or the like. The intermediate palladium layer acts as a diffusion barrier, and prevents the underlying nickel from diffusing into the uppermost gold layer.

The integrated circuit structure described above can be used to form relatively tight geometries, i.e., connection pads can be formed relatively close to each other without jeopardizing the reliability of the resulting integrated circuits. For example, integrated circuit structures made in this manner permit two adjacent connection pads to be disposed within 5 micrometers, or less, of each other.

In the preferred embodiment of the present invention, the Ni/Pd/Au metallization stack may have a nickel layer thickness ranging between .5 micrometers and 20 micrometers; a palladium

thickness ranging between .1 micrometers and 5 micrometers; and a gold layer thickness ranging between .03 micrometers and 2 micrometers.

Another aspect of the present invention relates to the process for forming such integrated circuit structure, and more particularly, to the process for forming the connection pads on the integrated circuit die during wafer level processing. The process includes the step of forming the patterned layer of interconnect metal upon a surface of the semiconductor wafer for electrically interconnecting the various semiconductor devices formed within each such integrated circuit die, as well as forming connection pads for making electrical connection to circuitry external to the semiconductor wafer. The process includes the step of forming a patterned layer of nickel by electroless plating over each connection pad for mechanically and electrically bonding to the interconnect metal at each such connection pad. Thereafter, the process forms a patterned layer of palladium by electroless plating over the patterned layer of nickel above each connection pad for preventing the nickel from out-diffusing through the palladium during subsequent heating cycles. Preferably, this palladium layer is plated directly onto the nickel layer without any intervening layer. A patterned layer of gold is then formed by electroless plating over the patterned layer of palladium above each connection pad to facilitate the joinder of such connection pad with a connection element, such as a solder bump or wire bond. This process permits connection pads to be disposed relatively closely to each other, e.g., within 5 micrometers of each other. If desired, the process may further include a thermal cycle heating step without causing the nickel layer to out-diffuse into the gold layer.

Brief Description of the Drawings

Fig. 1 is an a cross-sectional schematic view of a triple layer Ni/Pd/Au metal stack formed upon a copper metal interconnect layer on a bond pad of an integrated circuit, along with a gold bump secured thereto, in accordance with the present invention.

Fig. 2 is a partial top view of a semiconductor wafer illustrating identical integrated circuits formed upon such wafer, and further showing a series of connection pads formed upon each such integrated circuit.

Detailed Description of the Preferred Embodiments

Fig. 1 shows a cross-sectional view of an integrated circuit structure formed in accordance with the present invention. Semiconductor wafer 10 (the complete thickness of which is not visible in Fig. 1) is preferably a silicon wafer having an upper surface 11. Region 26 designates a copper interconnect metal region forming a connection pad; while connection pad 26 is shown as being made of copper, the interconnect metal could also be aluminum. Region 26 is surrounded by intermetal dielectric layer 15 which insulates interconnect metal conductors (like copper connection pad 26) from each other. A silicon passivation layer 13 is formed above the upper surface 12 of intermetal dielectric layer 15; as shown, a via or window is formed through silicon passivation layer 13 above copper connection pad 26.

Referring briefly to Fig. 2, semiconductor wafer 10 includes a number of identical integrated circuit die formed thereupon, including integrated circuit die 14, 16, 18, 20, 22, and 24. Each of these integrated circuit die have a series of semiconductor devices, such as MOS transistors (not shown), formed therein upon the surface 12 of semiconductor wafer 10 to form logic switches or other circuit components of an electronic circuit. Each such semiconductor device has two or more electrodes, or terminals (not shown), that need to be electrically interconnected with another circuit element, such as a power supply conductor, or perhaps the output terminal of a previous switch. In order to make such interconnections, one or more patterned layers of interconnect metal are applied over the upper surface 11 of semiconductor wafer 10; where two or more of such interconnect metal layers are used, an insulating layer, such as an oxide layer, is formed over the lower interconnect layer to insulate the upper interconnect layer therefrom. Through hole vias are formed when necessary to allow the upper interconnect layer to connect with the lower interconnect layer below.

As mentioned above, the metal interconnect layers have long been formed of aluminum, though copper is now being used to enhance the conductivity, reliability and speed of circuitry, especially for very fine line geometries used in advanced generations of integrated circuit technologies. Each integrated circuit includes a series of connection pads for making electrical connection to circuitry external to the integrated circuit. For example, one such connection pad might be coupled to a source of positive voltage, another might be coupled to ground, another might

receive an input control signal, and still another might be an output signal. In Fig. 1, one such connection pad is designated by reference numeral 26. Referring to Fig. 2, integrated circuit 14 includes a number of such connection pads, including two pads 28 and 30 that lie adjacent one another. The lowermost portions of such connection pads are initially formed by patterning the interconnect metal layer, which again may be copper, into a series of rectangles, or other shapes, that are not covered by any passivation layer.

In practicing the present invention, one or more wafers are fabricated through metal interconnect. Passivation layer 13 covers the interconnect metal, except for the connection pads 26, at which the interconnect metal (aluminum or copper) is exposed. A patterned layer of nickel is plated over each such connection pad for mechanically and electrically bonding to the underlying metal forming such connection pad. The plated nickel layer is "patterned" in the sense that it conforms to the pattern of the underlying interconnect metal connection pads. In Fig. 1, this nickel layer is identified by reference numeral 32 and is applied to a thickness of approximately 1.5 micrometers.

Nickel layer 32 is preferably applied using an electroless nickel deposition process at the wafer level. The wafers to be processed are placed into a cassette and cleaned using processes well known to those skilled in the art. The cassette of wafers is thereafter placed into a nickel plating tank and agitated. The plating time in the nickel tank is calculated based upon the targeted Ni thickness and the plating rate; the plating rate is a function of the temperature, pH, and nickel concentration. This plating rate can be determined by recording empirical data for known conditions of the temperature, pH, and nickel concentration of the plating bath. After the nickel layer has been plated to a thickness of approximately 0.5 micrometers, the cassette is removed from the nickel bath, and rinsed. It should be noted that the nickel layer is plated directly on top of the copper connection pads formed by the copper metal interconnect, without the need for any intervening layer of titanium or other material. Preferably, the thickness of the plated nickel layer ranges between 0.5 micrometers and 20 micrometers.

Following the creation of the nickel layer over the copper connection pads, the wafers are ready for plating of the palladium layer. In Fig. 1, this palladium layer is identified by reference

numeral 34 and is applied to a thickness of approximately 0.1 to 5 micrometers. Palladium layer 34 is preferably applied using an electroless deposition process at the wafer level. The wafers resulting from the nickel plating process described above are thereafter plated with Palladium by placing the wafer cassette into a tank containing a Palladium plating bath. Plating time in the Palladium tank is dependent upon the plating rate and the targeted Palladium thickness; this plating rate is a function of the temperature, pH and palladium concentration., and can be determined by recording empirical data for known conditions of the temperature, pH, and palladium concentration of the plating bath. The thickness of the plated layer of palladium preferably ranges between 0.1 micrometers and 5 micrometers.

Upon removal from the Palladium tank, the cassette is moved to the rinse tank to rinse away any remaining palladium bath solution. The resulting wafers now have a layer of palladium patterned according to the underlying pattern of nickel above each connection pad. As mentioned above, this palladium layer helps to prevent the nickel from diffusing outwardly into the gold during subsequent heating cycles.

The cassette containing the wafers is then placed into a tank containing a Gold plating bath, and is manually agitated for 12 minutes. The plated gold layer preferably has a thickness ranging between 0.03 micrometers and 2 micrometers.

At this point, the wafers have a patterned layer of gold plated over the patterned layer of palladium above each connection pad to facilitate the joinder of such connection pad with a connection element, such as a gold wire bond, solder ball, gold bump, nickel bump, etc. Referring to Fig. 1, this gold layer is identified by reference numeral 36. Upon removal from the Gold plating bath tank, the cassette is moved to the rinse tank to rinse off any remaining plating bath with cold rinse water. Finally, the resulting wafers are inspected for plating quality.

Because the triple metal stack of nickel, palladium, and gold can be plated over the copper connection pads so precisely in accordance with the method described above, the connection pads can be disposed within 5 micrometers of each other without imposing any process limitations. This allows the connection pads to be placed on a relatively small pitch, thereby facilitating the formation of a large number of connection pads on each integrated circuit die.

The process of the present invention includes the steps of forming such a triple metal stack above each connection pad, first by forming a patterned layer of nickel by electroless plating over each connection pad, then forming a patterned layer of palladium by electroless plating over the patterned layer of nickel, and finally forming a patterned layer of gold by electroless plating over the patterned layer of palladium.

Those skilled in the art will now appreciate that an improved integrated circuit structure has been described which is compatible with both copper and aluminum interconnect metal, and which facilitates the attachment of the integrated circuit connection pads to external circuitry a wide variety of attachment technologies, including gold wire bonds, solder bumps, gold bumps and nickel bumps, and without risk of the nickel layer out-diffusing into the upper gold layer during subsequent heat cycling. For example, within Fig. 1, a gold bump or ball 38 has been affixed to gold layer 36 atop connection pad 26 to facilitate the joinder of such connection pad to a supporting substrate or package. The described electroless plating technique can be practiced at the wafer level, is relatively simple, yet precise, allowing small pitch geometries for tight placement of the connection pads. Moreover, connection pads provided with the aforementioned plated triple metal stack have been found to permit the use of temporary test probes for testing purposes prior to final packaging, but without harm to the connection pads. Those skilled in the art will also appreciate that an improved process has been described for providing such connection pads .

While the present invention has been described with respect to preferred embodiments thereof, such description is for illustrative purposes only, and is not to be construed as limiting the scope of the invention. Various modifications and changes may be made to the described embodiments by those skilled in the art without departing from the true spirit and scope of the invention as defined by the appended claims.